Laboratory Report

ECSE-431

Introduction to VLSI CAD

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# Description of design

Figure 1 – Layout of the blocks used in our circuit

Timer +

Comparator

Register

Timer +

Comparator

Nios\_2

* - Description of design that highlights important aspects (10 pts):   
  -- Include diagrams that illustrate the functioning of the main circuit components. \*Clean\* hand-drawn diagrams are acceptable (in electronic form).

-- Please also describe the operation of any FSM, either graphically or using a table of some sort.

# Validation methodology

Table 1 – List of requirements, tests and results

|  |  |  |
| --- | --- | --- |
| **Requirements** | **Tests** | **Results** |
| Reset |  |  |
| Register read/write |  |  |
| Register read/write-to-clear |  |  |
| Pulse from timers sets proper registers |  |  |
| Counters (count and compare) |  |  |
| Interrupts (0 and 1) |  |  |
| Count of interrupts on GP0 |  |  |
| Polling vs Avalon int |  |  |
| Interrupts off |  |  |

* - Validation methodology (10 pts): Should be in the form of  requirement -> test -> expected result.

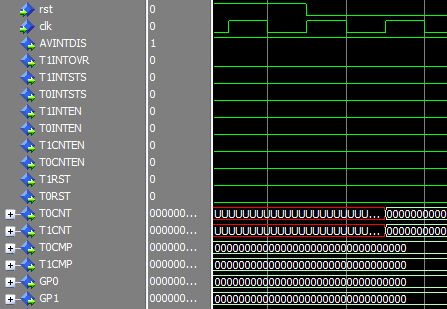
# Synthesis and P&R reports

According to TimeQuest Timing Analyzer, the critical path of our circuit is from the node M\_rot\_rn[2] to the node to Mn\_rot\_step2[13] of the CPU. The slack of this path is 6.856 ns. Since this number is positive, we should not encounter problems due to the frequency of our clock. Technically, we could reduce the period of the clock by the slack without causing problems to the compiler.

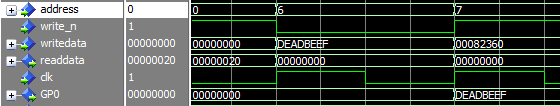


Appendix

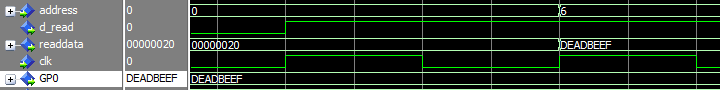
Test 0: Reset



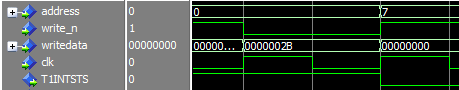
Test 1: Shows write of 0xDEADBEEF to GP0



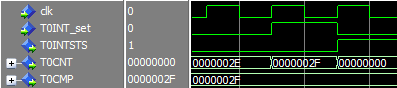
Test 1 : Show read of GP0



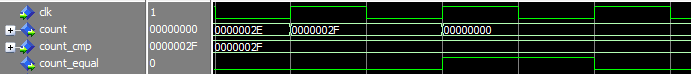
Test 2: Write to clear



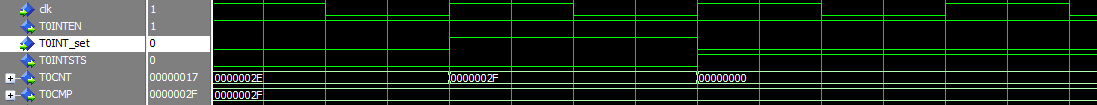
Test 4: Pulse from counter sets register



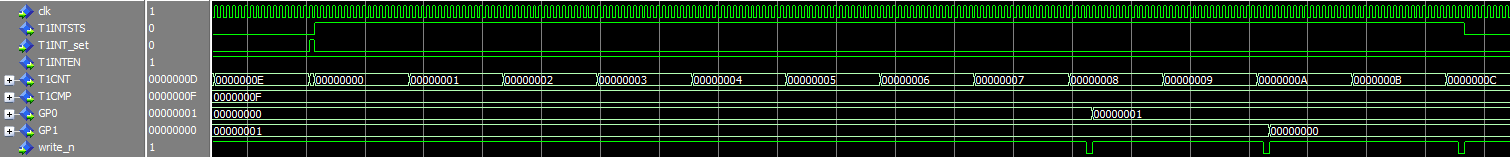
Test 5: Counters



Test 6: Interrupt on 0



Test 7: Interrupt on 1, GP0 increases by 1, ISR



Test 8: Full GP0 count

